TERIDIAN SEMICONDUCTOR CORP.

73S8010C Smart Card Interface

Simplifying System Integration™

DATA SHEET

ISO/IEC 7816-3 EMVCo

April 2009

DESCRIPTION

The Teridian 73S8010C is a single smart card interface IC. It provides full electrical compliance with ISO-7816-3 and EMV 4.0 specifications.

Interfacing with the host is done through the two-wire I2C bus. Data exchange with the card is managed from the system controller using the I/O line (and eventually the auxiliary I/O lines).

An on-chip oscillator using an external crystal, or connection to a clock signal coming from the system controller can generate the card clock signal.

The 73S8010C IC incorporates an ISO-7816-3 activation/deactivation sequencer that controls the card signals. Level shifters drive the card signals with the selected card voltage (3 V or 5 V), coming from an internal DC-DC converter.

With its high-efficiency DC-DC converter, the Teridian 73S8010C is a cost-effective solution for any smart card reader application to be powered from a single 2.7 V to 3.6 V power supply.

Hardware support for auxiliary I/O lines, C4 / C8 contacts, is provided.

Emergency card deactivation is initiated upon card extraction or upon any fault generated by the protection circuitry. The fault can be a VDD (digital power supply), a VCC (card power supply), a card over-current, or an over-heating fault.

ADVANTAGES

- Single smart card interface
- The inductor-based DC-DC converter provides higher current and efficiency than the usual charge-pump capacitor-based converters
  - → Ideal for battery-powered applications
  - → Suitable for high current cards and SAMs: (100 mA max)
- Power down mode: 2 µA typical
- Small Format (5x5mm) 32-QFN package option

FEATURES

- **Card Interface:**
  - Complies with ISO-7816-3 and EMV 4.0
  - A DC-DC Converter provides 3V / 5V to the card from an external power supply input
  - High-efficiency converter: > 80% @ V_{DD}= 3.3 V, V_{CC} = 5 V and I_{CC} = 65 mA
  - Up to 100 mA supplied to the card
  - ISO-7816-3 Activation / Deactivation sequencer with emergency automated deactivation on card removal or fault detected by the protection circuitry
  - Protection include 2 voltage supervisors that detect voltage drops on card V_{CC} and V_{DD} power supplies
  - The V_{DD} voltage supervisor threshold value can be externally adjusted
  - True over-current detection (150 mA max.)
  - 1 card detection input
  - Auxiliary I/O lines, for C4 / C8 contact signals
- **Host Interface:**
  - Fast mode, 400 kbps I^2C slave bus
  - 8 possible devices in parallel
  - One control register and one status register
  - Interrupt output to the host for fault detection
  - Crystal oscillator or host clock, up to 27 MHz
- **Power Supply:**
  - V_{DD}: 2.7 V to 3.6 V
- **6 kV ESD Protection on the card interface**
- **Package: SO28 or 32QFN**

APPLICATIONS

- Set-Top-Boxes, DVD / HDD Recorders: Conditional Access and Pay-per-View slots
- Point of Sales and Transaction Terminals
- EMV slots in cell phones and PDAs

FUNCTIONAL DIAGRAM

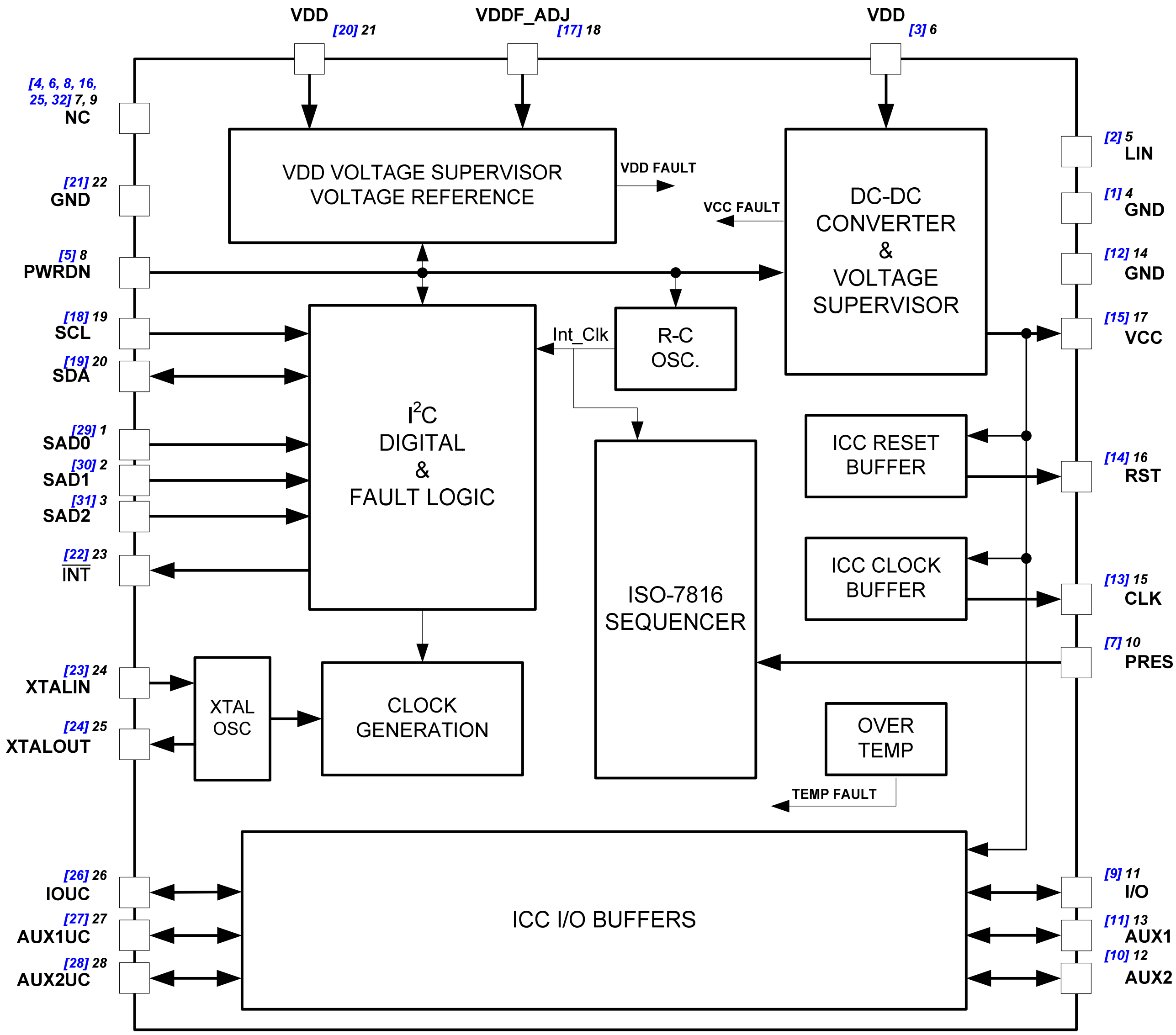


Figure 1: 73S8010C Block Diagram

Pin number reference to SO28 Package

[Pin number] reference to 32QFN Package

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Tables

1 Pin Description

1.1 Card Interface

Name	Pin (SO)	PIN (QFN)	Description
I/O	11	9	Card I/O: Data signal to/from card. Includes a pull-up resistor to $V_{CC.}$
AUX1	13	11	AUX1: Auxiliary data signal to/from card. Includes a pull-up resistor to $V_{CC.}$
AUX2	12	10	AUX2: Auxiliary data signal to/from card. Includes a pull-up resistor to $V_{CC.}$
RST	16	14	Card reset: provides reset (RST) signal to card.
CLK	15	13	Card clock: provides clock (CLK) signal to card. The rate of this clock is determined by the crystal oscillator frequency and CLKSEL bits in the control register.
PRES	10	7	Card Presence switch: active high indicates card is present. Includes a pull-down resistor.
VCC	17	15	Card power supply: logically controlled by sequencer, output of DC-DC converter. Requires an external filter capacitor to the card GND.
GND	14	12	Card ground.

1.2 Miscellaneous Inputs and Outputs

Name	PIN (SO)	PIN (QFN)	Description
XTALIN	24	23	Crystal oscillator input: can either be connected to a crystal or driven as a source for the card clock.
XTALOUT	25	24	Crystal oscillator output: connected to crystal. Left open if XTALIN is being used as an external clock input.
VDDF_ADJ	18	17	V_{DD} threshold adjustment input: this pin can be used to overwrite a higher V_{DDF} value (that controls deactivation of the card). Must be left open if unused.
NC	7, 9	4, 6, 8, 16, 25, 32	Non-connected pin.

1.3 Power Supply and Ground

Name	PIN (SO)	Pin (QFN)	Description
VDD	6, 21	3, 20	System controller interface supply voltage: supply voltage for internal circuitry and DC-DC converter power supply source.
GND	4	1	DC-DC converter ground.
GND	14	12	Smart Card I/O ground.
GND	22	21	Digital ground.
LIN	5	2	External inductor: Connect external inductor from pin 5 to V_{DD}. Keep the inductor close to pin 5.

1.4 Microcontroller Interface

<table>
<tr><th>Name</th><th>PIN (SO)</th><th>PIN (QFN)</th><th>Description</th></tr>
<tr><td>INT</td><td>23</td><td>22</td><td>Interrupt output (negative assertion): Interrupt output signal to the processor. A 20 kΩ pull up to V_{DD} is provided internally.</td></tr>
<tr><td>PWRDN</td><td>8</td><td>5</td><td>Power Down control input: Active High. When Power Down (PD) mode is activated, all internal analog functions are disabled to place the 73S8010C in its lowest power consumption mode. Must be tied to ground when the power down function is not used.</td></tr>
<tr><td>SAD0
SAD1
SAD2</td><td>1
2
3</td><td>29
30
31</td><td>Serial device address bits: Digital inputs for address selection that allow the connection of up to 8 devices in parallel. Address selections as follows:
<table>
<tr><th>SAD2</th><th>SAD1</th><th>SAD0</th><th>I²C Address (7 bits)</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0x40</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0x42</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>0x44</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0x46</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0x48</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0x4A</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>0x4C</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0x4E</td></tr>
</table>
Pins SAD0 and SAD1 are internally pulled-down and SAD2 is internally pulled-up.
The default address when left unconnected is 48h.</td></tr>
<tr><td>SCL</td><td>19</td><td>18</td><td>I²C clock signal input.</td></tr>
<tr><td>SDA</td><td>20</td><td>19</td><td>I²C bi-directional serial data signal.</td></tr>
<tr><td>I/OUC</td><td>26</td><td>26</td><td>System controller data I/O to/from the card. Includes internal pull-up resistor to V_{DD}.</td></tr>
<tr><td>AUX1UC</td><td>27</td><td>27</td><td>System controller auxiliary data I/O to/from the card. Includes internal pull-up resistor to V_{DD}.</td></tr>
<tr><td>AUX2UC</td><td>28</td><td>28</td><td>System controller auxiliary data I/O to/from the card. Includes internal pull-up resistor to V_{DD}.</td></tr>
</table>

2 Host Interface (I^2C Bus)

A fast-mode 400 kHz I^2C bus slave interface is used for controlling the device and reading the status of the device via the data pin SDA and clock pin SCL. The bus has 3 address select pins, SAD0, SAD1, and SAD2. This allows up to 8 devices to be connected in parallel.

Table 1: Device Address Selections

SAD2	SAD1	SAD0	I^2C Address (7 bits)
0	0	0	0x40
0	0	1	0x42
0	1	0	0x44
0	1	1	0x46
1	0	0	0x48
1	0	1	0x4A
1	1	0	0x4C
1	1	1	0x4E

Bit 0 of the I^2C address is the R/W bit. Refer to Figure 2 and Figure 3 for usage.

2.1 Host Interface Control

Table 2 describes the Host Interface Control Register bits (power-on Reset = 0x00).

Table 2: Host Control Register

<table>
<tr><th>Name</th><th>Bit</th><th>Description</th></tr>
<tr><td>Start/Stop</td><td>0</td><td>When set, initiates an activation and a cold reset procedure; when reset, initiates a deactivation sequence.</td></tr>
<tr><td>Warm reset</td><td>1</td><td>When set, initiates a warm reset procedure; automatically reset by hardware when the card starts answering or when the card is declared mute.</td></tr>
<tr><td>5 V and 3 V</td><td>2</td><td>When set, V_{CC} = 3 V; when reset, V_{CC} = 5 V.</td></tr>
<tr><td>Clock Stop</td><td>3</td><td>When set, card clock is stopped. Bit 4 determines the card clock stop level.</td></tr>
<tr><td>Clock Stop Level</td><td>4</td><td>When set, card clock stops high; when reset card clock stops low.</td></tr>
<tr><td>Clksel1</td><td>5</td><td rowspan="2">Bits 5 and 6 determine the clock rate to the card according to the following table.
<table>
<tr><th>CLKDIV1</th><th>CLKDIV2</th><th>Clock Rate</th></tr>
<tr><td>0</td><td>0</td><td>XTALIN/8</td></tr>
<tr><td>0</td><td>1</td><td>XTALIN/4</td></tr>
<tr><td>1</td><td>1</td><td>XTALIN/2</td></tr>
<tr><td>1</td><td>0</td><td>XTALIN</td></tr>
</table></td></tr>
<tr><td>Clksel2</td><td>6</td></tr>
<tr><td>I/O enable</td><td>7</td><td>When set, data is transferred between I/O (AUX1, AUX2) and I/OUC (AUX1UC, AUX2UC); when reset, I/O (AUX1, AUX2) and I/OUC (AUX1UC, AUX2UC) are high impedance.</td></tr>
</table>

I^2C-bus Write to the Control Register

The I^2C-bus Write command to the control register follows the format shown in Figure 2.

After the START condition, the master sends a slave address. This address is seven bits long followed by an eighth bit, which is an opcode bit (R/W) – a 'zero' indicates the master will write data to the control register. After the R/W bit, the 'zero' ACK bit is sent to the master by the device. The master now starts sending the 8 bits of data to the control register during the DATA bits time. After the DATA bits, the 'zero'

ACK bit is sent to the master by the device. The master should send the STOP condition after receiving the ACK bit.

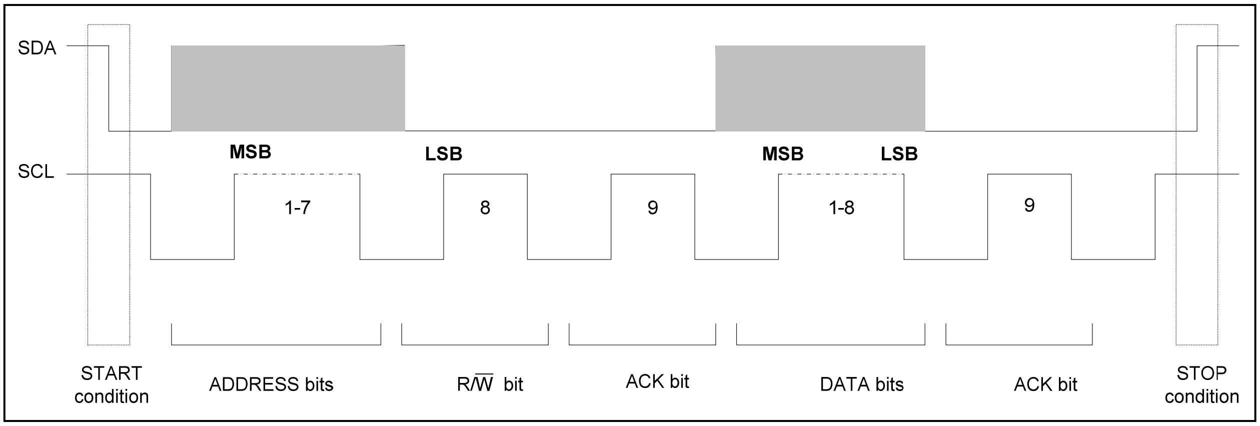


Figure 2: I^{2}C Bus Write Protocol

2.2 Host Interface Status

Table 3 describes the Host Interface Status Register bits (power-on Reset = 0x04).

Table 3: Host Status Register

Name	Bit	Description
PRES	0	Set when the card is present; reset when the card is not present.
PRESL	1	Set when the PRES pin changes state (rising/falling edge); reset when the status register is read. Generates an interrupt when set
I/O	2	Set when I/O is high; reset when I/O is low.
SUPL	3	Set when a voltage fault is detected; reset when the status register is read. Generates an interrupt when set.
PROT	4	Set when an over-current or over-heating fault has occurred during a card session; reset when the status register is read. Generates an interrupt when set.
MUTE	5	Set during ATR when the card has not answered during the ISO 7816-3 time window (40000 card clock cycles); reset when the next session begins or this register is read.
EARLY	6	Set during ATR when the card has answered before 400 card clock cycles; reset when the next session begins or this register is read.
ACTIVE	7	Set when the card is active (V_{CC} is on); reset when the card is inactive.

I^{2}C-bus Read from the Status Register:

The I^{2}C-bus Read Command from the Status Register follows the format shown in Figure 3.

After the START condition, the master sends a slave address. This address is seven bits long followed by an eighth bit, which is the opcode bit (R/$\overline{W}$). A 'one' indicates the master will read data from the status register. After the R/$\overline{W}$ bit, the 'zero' ACK bit is sent to the master by the device. The device now starts sending the 8-bit status register data to the control register during the DATA bits time. After the DATA bits, the 'one' ACK bit is sent to the device by the master. The master should send the STOP condition after receiving the ACK bit.

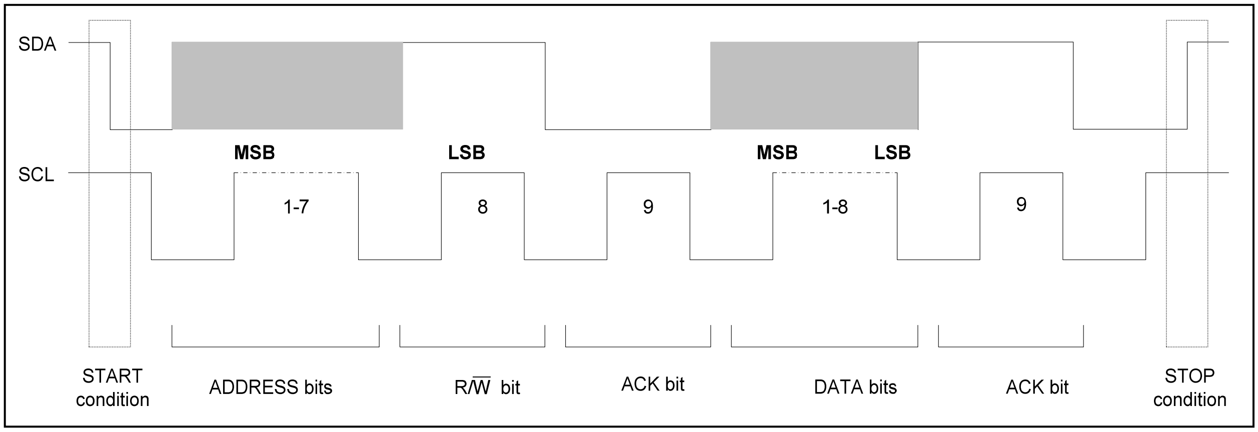


Figure 3: I²C Bus Read Protocol

2.3 I²C-bus Timing

Symbol	Parameter	Conditions	Min.	Typ.	Max.	UNIT
Fsclk	Clock frequency				400	kHz
Tlow	Clock low		1.3			µs
Thi	Clock high		0.6			µs
Thdsta	Hold time START condition		0.6			µs
Tsudat	Data set up time		100			ns
Thddat	Data hold time		5		900	ns
Tsusto	Set up time STOP condition		0.6			µs
Tbuf	Bus free time between a STOP and START condition		1.3			µs

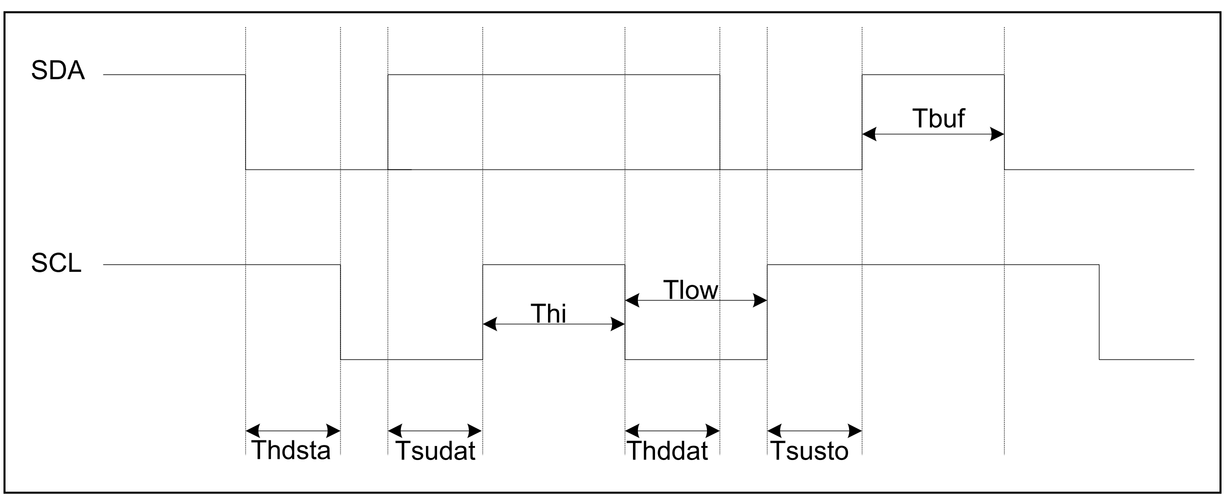


Figure 4: I²C Bus Timing Diagram

3 Oscillator

The Teridian 73S8010C device has an on-chip oscillator that can generate the smart card clock using an external crystal, connected between the XTALIN and XTALOUT pins, to set the oscillator frequency. When the card clock signal is available from another source, it can be connected to the pin XTALIN, and the pin XTALOUT should be left unconnected.

4 DC-DC Converter – Card Power Supply

An internal DC-DC converter provides the card power supply. This converter is able to provide either a 3 V or 5 V card voltage from the power supply applied on the V_{DD} pin. The digital ISO-7816-3 sequencer controls the converter. Bit 2 of the Control register selects the card voltage.

The circuit is an inductive step-up converter/regulator. The external components required are 2 filter capacitors on the power-supply input V_{DD} (100 nF + 10 μF, next to the LIN pin), an inductor, and an output filter capacitor on the card power supply V_{CC}. The circuit performs regulation by activating the step-up operation when V_{CC} is below a set point of 5.0 or 3.0 volts minus a comparator hysteresis voltage and the input supply V_{DD} is less than the set point for V_{CC}. When V_{DD} is greater than the set point for V_{CC} (V_{DD} = 3.6 V, V_{CC} = 3 V) the circuit operates as a linear regulator. Depending on the inductor values, the voltage converter can provide current on V_{CC} as high as 100 mA.

The circuit provides over-current protection and limits I_{CC} to 150 mA. When an over-current condition is sensed, the circuit initiates a deactivation sequence from the control logic and reports back to the host controller a fault on the interrupt output $\overline{INT}$.

Choice of the Inductor

The nominal inductor value is 10 μH, rated for 400 mA. The inductor is connected between pin LIN (pin 5 in the SO package, pin 2 in the QFN package) and the V_{DD} voltage. The value of the inductor can be optimized to meet a particular configuration (I_{CC_MAX}). The inductor should be located on the PCB as close as possible to the LIN pin of the IC.

Choice of the V_{CC} Capacitor

Depending on the applications, the requirements in terms of both V_{CC} minimum voltage and transient currents that the interface must be able to provide to the card vary. Table 4 shows the recommended capacitors for each V_{CC} power supply configuration and applicable specification.

Table 4: Choice of Vcc Capacitor

Specification Requirement			Application	
Specification	**Min V_{CC} Voltage Allowed During Transient Current**	**Max Transient Current Charge**	**Capacitor Type**	**Capacitor Value**
EMV 4.0	4.6V	30nA.s	X5R/X7R w/ ESR < 100 mΩ	3.3 μF
ISO-7816-3	4.5V	20nA.s		1 μF

5 Voltage Supervision

Two voltage supervisors constantly check the level of the V_{DD} and V_{CC} voltages. A card deactivation sequence is forced when a fault occurs for any of these voltage supervisors.

The digital circuitry is powered by the power supply applied on the VDD pin. V_{DD} also defines the voltage range to interface with the system controller. The V_{DD} voltage supervisor is also used to initialize the ISO-7816-3 sequencer at power-on, and to deactivate the card at power-off or when a fault occurs. The voltage threshold of the V_{DD} voltage supervisor is internally set by default to 2.3 V nominal. However, it may be desirable in some applications, to modify this threshold value. The pin VDDF_ADJ (pin 18 in the SO package, pin 17 in the QFN package) is used to connect an external resistor R_{EXT1} to ground to raise the V_{DD} fault voltage to another value, V_{DDF} (refer to Figure 11). The resistor value is defined as follows:

R_{EXT} = 180 kΩ / (V_{DDF} - 2.33)

An alternative (more accurate) method of adjusting the V_{DD} fault voltage is to use a resistive network of R3 from the pin to supply and R4 from the pin to ground (see Figure 11). In order to set the new threshold voltage, the equivalent resistance must be determined. This resistance value will be designated Kx. Kx is defined as R4/(R4+R5). Kx is calculated as:

Kx = (2.649 / V_{TH}) - 0.6042 where V_{TH} is the desired new threshold voltage.

To determine the values of R4 and R5, use the following formulas.

R5 = 72000 / Kx R4 = R5*(Kx / (1 – Kx))

Taking the example above, where a V_{DD} fault threshold voltage of 2.7 V is desired, solving for Kx gives:

→ Kx = (2.649 / 2.7) - 0.6042 = 0.377.

Solving for R5 gives: → R5 = 72000 / 0.377 = 191 kΩ.
Solving for R4 gives: → R4 = 191000 *(0.377 / (1 – 0.377)) = 115.6 kΩ.

Using standard 1% resistor values gives R5 = 191 kΩ and R4 = 115 kΩ. These values give an equivalent resistance of Kx = 0.376, a 0.3% error.

If the 2.3 V default threshold is used, the VDDF_ADJ pin must be left unconnected.

6 Power Down

A power down function is provided via the PWRDN pin (active high). When activated, the Power Down (PD) mode disables all the internal analog functions, including the card analog interface, the oscillators and the DC-DC converter, to put the 73S8010C in its lowest power consumption mode. PD mode is only allowed in the deactivated condition (out of a card session, when the Start/Stop bit is set to 0 from the I^2C host controller).

The host controller invokes the power down state when it is desirable to save power. The signal PRES remains functional in PD mode such that a card insertion sets $\overline{INT}$ high. The micro-controller must then set PWRDN low and wait for the internal stabilization time prior to starting any card session (prior to setting the Start/Stop bit to 1).

Resumption of the normal mode occurs approximately 10 ms (stabilization of the internal oscillators + reset of the circuitry) after PWRDN is set low. No card activation should be invoked during this 10 ms time period. If a card is present, $\overline{INT}$ can be used as an indication that the circuit has completed its recovery from power down state. $\overline{INT}$ will go high at the end of the stabilization period. Should the Start/Stop be set to 1 during PWRDN = 1, or within the 10 ms internal stabilization / reset time, it will not be taken into account and the card interface will remain inactive. Since Start/Stop is taken into account on its edges, it should be toggled low and high again after the 10 ms to activate a card.

Figure 5 illustrates the sequencing of the PD and Normal modes. PWRDN must be connected to GND if the power down function is not used.

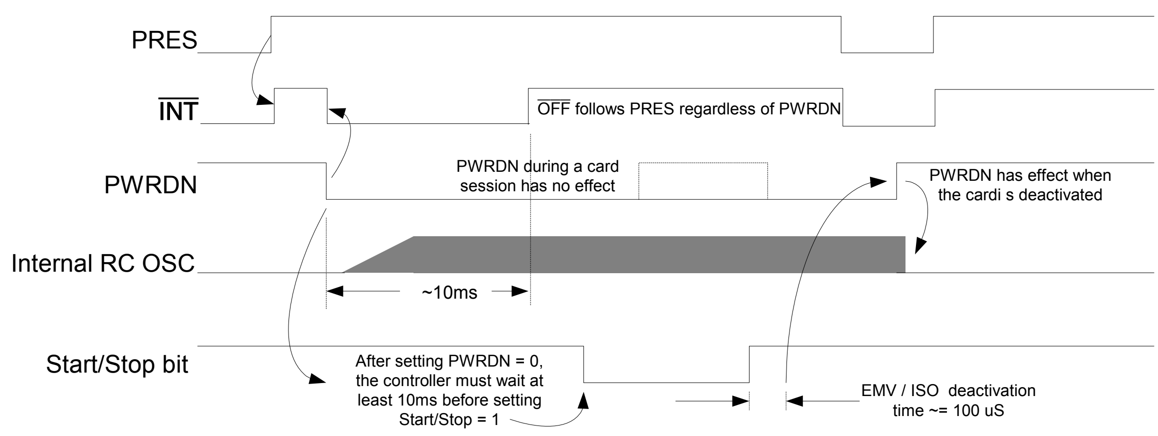


Figure 5: Power Down Mode Operation

7 Over-temperature Monitor

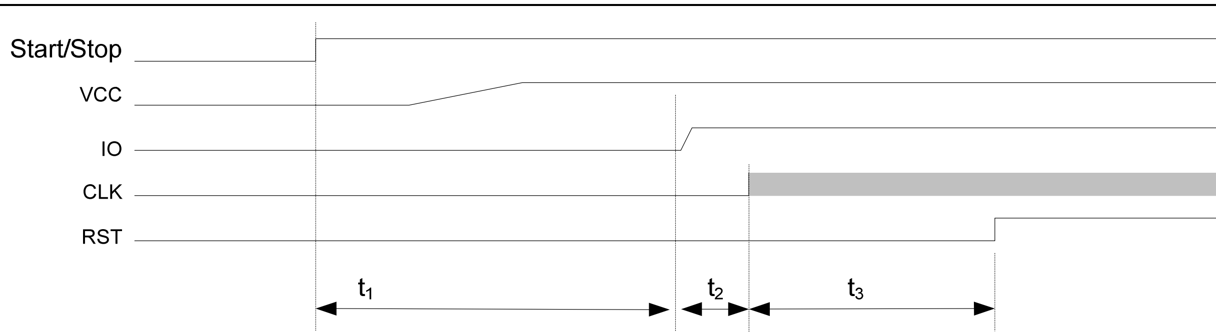
A built-in detector monitors die temperature. When an over-temperature condition occurs (most likely resulting from a heavily loaded card interface, including short circuits), a card deactivation sequence is initiated, and a fault condition is reported to the system controller (bit 4 of the status register is set and generates an interrupt).

8 Activation Sequence

After Power on Reset, the $\overline{INT}$ signal is low until V_{DD} is stable. When V_{DD} has been stable for approximately 10 ms and the $\overline{INT}$ signal is high, the system controller may read the status register to see if the card is present. If all the status bits are satisfactory, the system controller can initiate the activation sequence by writing a '1' to the Start/Stop bit (bit 0 of the Control register).

The following steps and Figure 6 show the activation sequence and the timing of the card control signals when the system controller initiates the Start/Stop bit (bit 0) of the control register:

1. Voltage V_{CC} to the card should be valid by the end of t_1. If V_{CC} is not valid for any reason, then the session is aborted.
2. Turn I/O to reception mode at the end of t_1.
3. CLK is applied to the card at the end of t_2.
4. RST (to the card) is set high at the end of t_3.



t_1 = 0.510 ms (timing by 1.5 MHz internal Oscillator), I/O in reception mode
$t_2 \geq$ 0.5 µs, CLK starts
$t_3 \geq$ 42000 card clock cycles, RST set high

Figure 6: Activation Sequence

9 Deactivation Sequence

Deactivation is initiated either by the system controller resetting the Start/Stop bit, or automatically in the event of hardware faults. Hardware faults are over-current, over-temperature, V_{DD} fault, V_{CC} fault, and card extraction during the session.

The following steps and Figure 7 show the deactivation sequence and the timing of the card control signals when the system controller clears the Start/Stop bit:

1. RST goes low at the end of t_1.
2. CLK goes low at the end of t_2.
3. I/O goes low at the end of t_3. Out of reception mode.
4. Shut down V_{CC} at the end of time t_4.

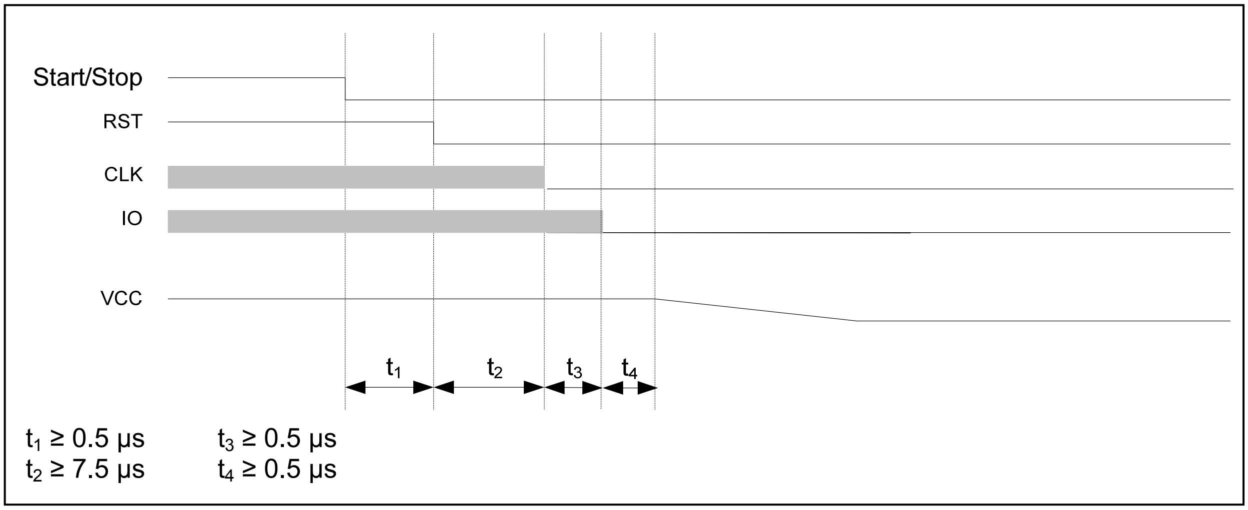


Figure 7: Deactivation Sequence

10 Interrupt

The interrupt is an active low interrupt. It is set low if either a V_{CC} fault or a V_{DD} fault is detected. It is also set low if one of the following status bit conditions is detected:

- Early ATR
- Mute ATR
- Card insert or card extract
- Protection status from Over-current or Over-heating

If the interrupt is set low by the detection of these status bits, then the interrupt is set high when these status bits are read. (READ STATUS DONE)

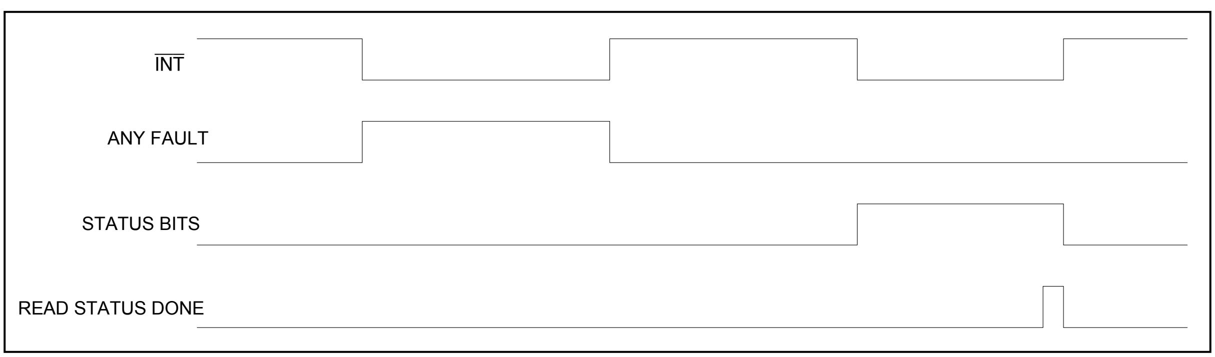
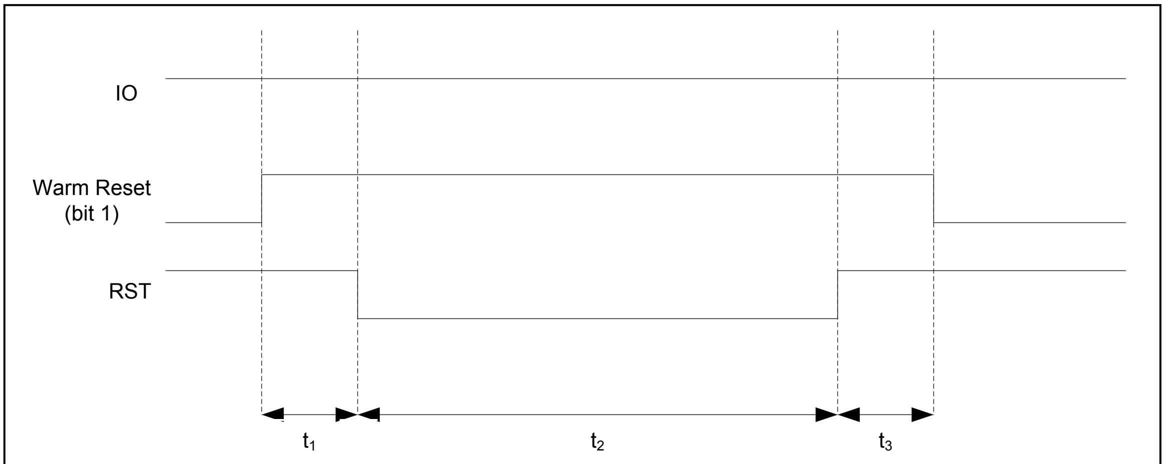


Figure 8: FAULT Functions, $\overline{INT}$ operation

A power-on-reset (POR) event will reset all of the control and status registers to their default states. A V_{DD} fault event does not reset these registers, but it will signal an interrupt condition and by the action of the timer that creates interval "t_1," will not clear the interrupt until V_{DD} is valid for at least the t_1 time. The V_{DD} fault can be considered valid for V_{DD} as low as 1.5 to 1.8 volts. At the lower range of the V_{DD} fault, POR will be asserted.

11 Warm Reset

The 73S8010C automatically asserts a warm reset to the card when instructed through bit 1 of the I^2C Control register (Warm Reset bit). The warm reset length is automatically defined as 42,000 card clock cycles. The bit Warm Reset is automatically reset when the card starts answering or when the card is declared mute.



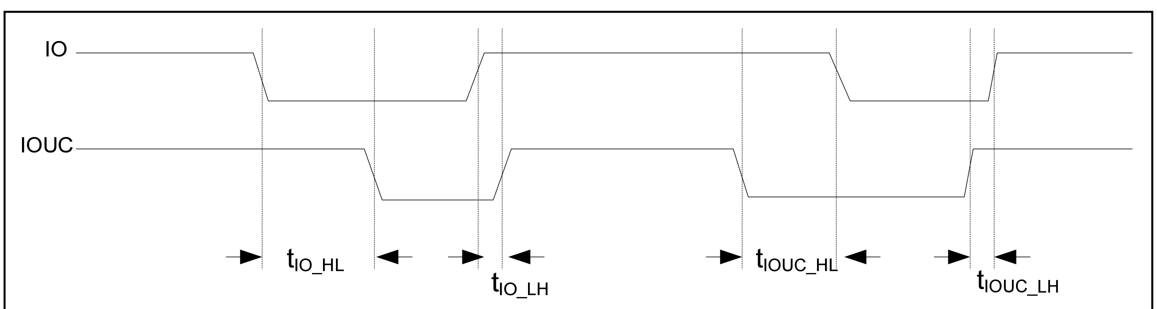
t_1 > 1.5 µs, Warm Reset Starts
t_2 = 42000 card clock cycles, End of Warm Reset
t_3 = Resets Warm Reset bit 1 when detected ATR or Mute

Figure 9: Warm Reset operation

12 I/O Timing

The states of the I/O, AUX1, and AUX2 pins are low after power on reset and they are high when the activation sequencer turns on the I/O reception state. See Section 8 Activation Sequence for more details on when the I/O reception is enabled.

The states of I/OUC, AUX1UC, and AUX2UC are high after power on reset. When the control I/O enable bit (bit 7 of the Control register) is set, the first I/O line on which a falling edge is detected becomes the input I/O line and the other becomes the output I/O line. When the input I/O line rising edge is detected then both I/O lines return to their neutral state. The delay between the I/O signals is shown in Figure 10.



Delay from I/O to I/OUC: t_{IO_HL} = 100 ns t_{IO_LH} = 25 ns
Delay from I/OUC to I/O: t_{I/OUC_HL} = 100 ns t_{I/OUC_LH} = 25 ns

Figure 10: I/O Timing

13 Typical Application Schematic

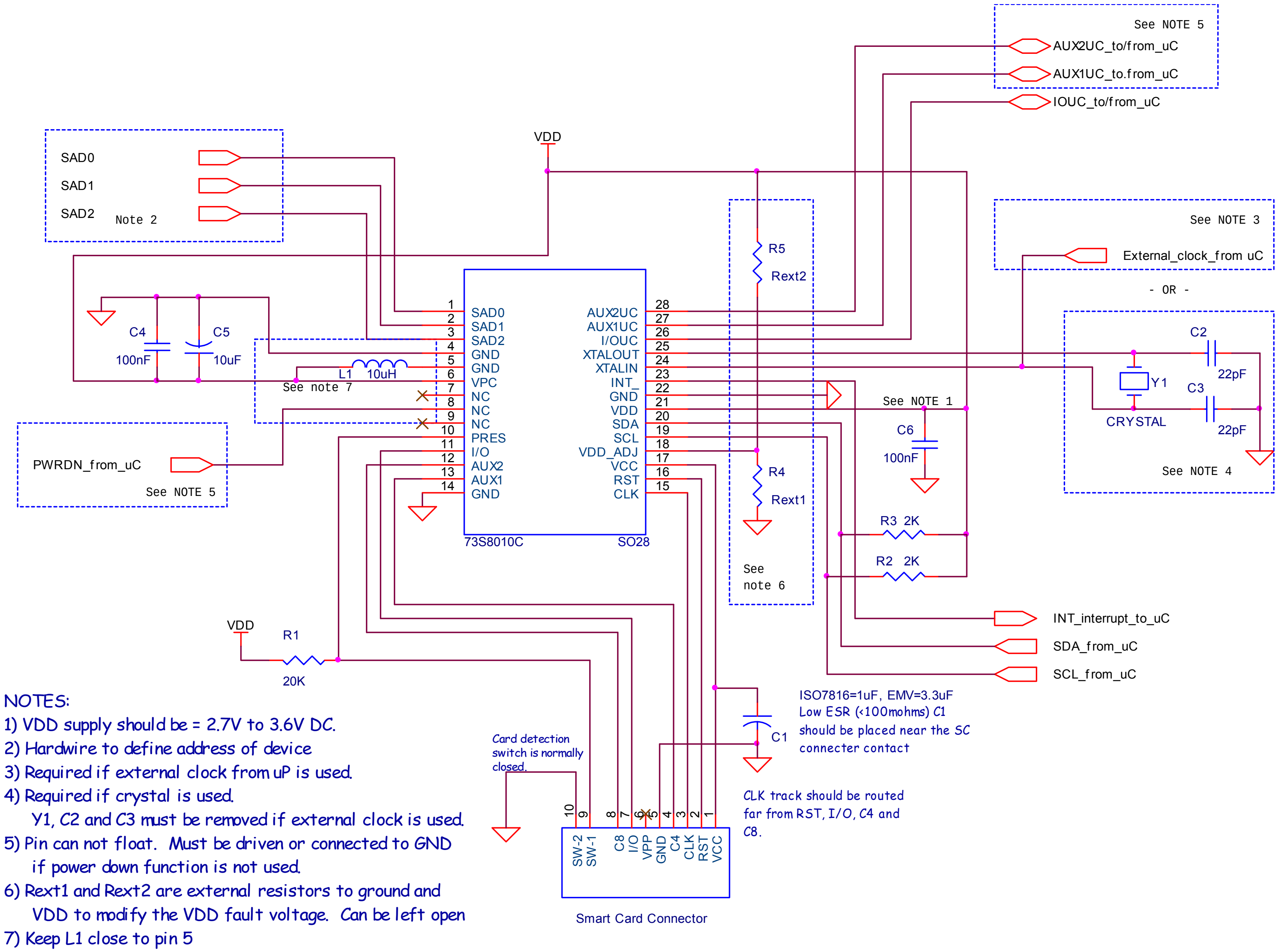


Figure 11: 73S8010C – Typical Application Schematic

14 Electrical Specification

14.1 Absolute Maximum Ratings

Operation outside these rating limits may cause permanent damage to the device.

Parameter	Rating
Supply Voltage V_{DD}	-0.5 to 4.0 VDC
Input Voltage for Digital Inputs	-0.3 to (V_{DD} +0.5) VDC
Storage Temperature	-60 °C to 150 °C
Pin Voltage (except LIN and card interface)	-0.3 to (V_{DD} +0.5) VDC
Pin Voltage (LIN)	-0.3 to 6.0 VDC
Pin Voltage (card interface)	-0.3 to (V_{CC} + 0.5) VDC
ESD Tolerance – Card interface pins	+/- 6 kV
ESD Tolerance – Other pins	+/- 2 kV

ESD testing on Card pins uses the HBM condition, 3 pulses, each polarity referenced to ground.

14.2 Recommended Operating Conditions

Parameter	Rating
Supply Voltage V_{DD}	2.7 to 3.6 VDC
Ambient Operating Temperature	-40 °C to +85 °C
Input Voltage for Digital Inputs	0 V to V_{DD} + 0.3 V

14.3 DC Characteristics: Card Interface

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Card Power Supply (V_{CC}) DC-DC Converter **General conditions, -40 °C < T < 85 °C, 2.7 V < V_{DD} < 3.6 V**						
V_{CC}	Card supply voltage including ripple and noise	Inactive mode	-0.1		0.1	V
		Inactive mode I_{CC} = 1 mA	-0.1		0.4	V
		Active mode I_{CC} < 65 mA; 5 V	4.75		5.25	V
		Active mode I_{CC} < 65 mA; 3 V	2.8		3.2	V
		Active mode single pulse of 100 mA for 2 µs; 5 V, fixed load = 25 mA	4.6		5.25	V
		Active mode single pulse of 100 mA for 2 µs; 3 V, fixed load = 25 mA	2.76		3.2	V
		Active mode current pulses of 40 nAs with peak $\|I_{CC}\|$ < 200 mA, t < 400 ns; 5 V	4.6		5.25	V
		Active mode current pulses of 40 nAs with peak $\|I_{CC}\|$ < 200 mA, t < 400 ns; 3 V	2.76		3.2	V
I_{CCmax}	Maximum supply current to the card	Static load current, V_{CC} > 4.6 or 2.7 V as selected, L=10 µH	100			mA
I_{CCF}	I_{CC} fault current	Short circuit, V_{CC} to ground	100	125	180	mA
V_{SR}	V_{CC} slew rate - Rise rate on activate	C_F on V_{CC} = 1 µF	0.05	0.15	0.25	V/µs
V_{SF}	V_{CC} slew rate - Fall rate on deactivate	C_F on V_{CC} = 1 µF	0.1	0.3	0.5	V/µs
C_F	External filter capacitor (V_{CC} to GND)		0.47	1	3.3	µF
L	Inductor (LIN to V_{DD})			10		µH
Limax	Imax in inductor	V_{CC} = 5 V, I_{CC} = 65 mA, V_{DD} = 2.7 V			400	mA
η	Efficiency	V_{CC} = 5 V, I_{CC} = 65 mA, V_{DD} = 3.3 V		87		%

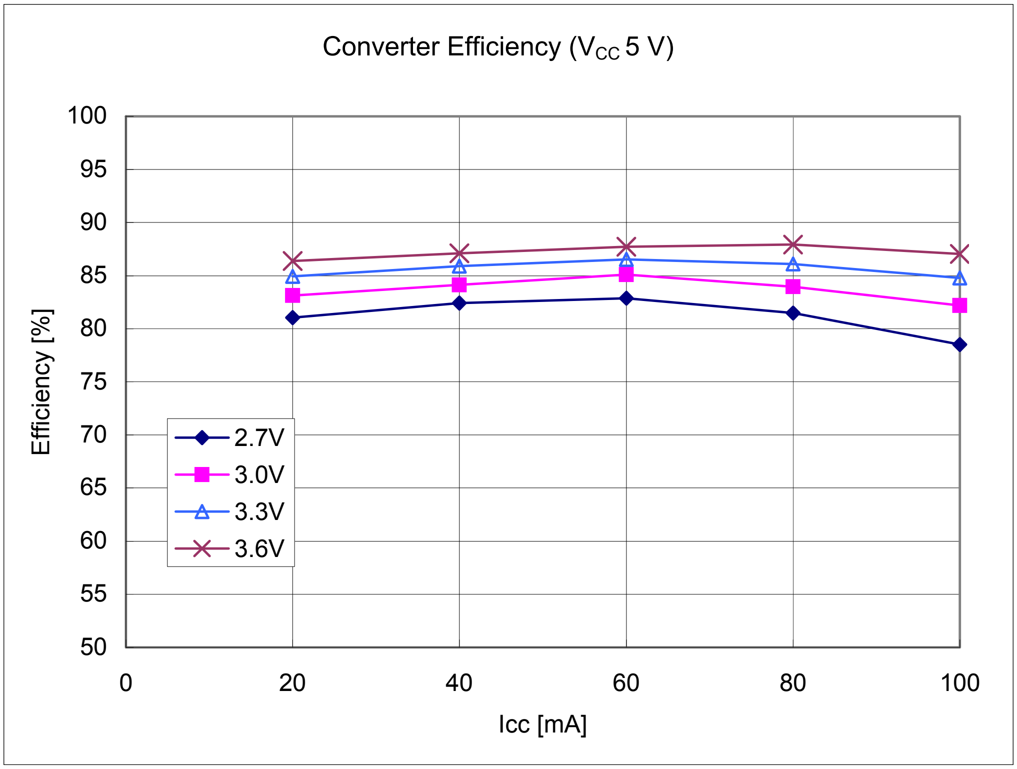


Figure 12: DC – DC Converter Efficiency (V_{CC} = 5 V)

Output current on Vcc at 5 V. Input voltage on V_{DD} at 2.7, 3.0, 3.3 and 3.6 volts.

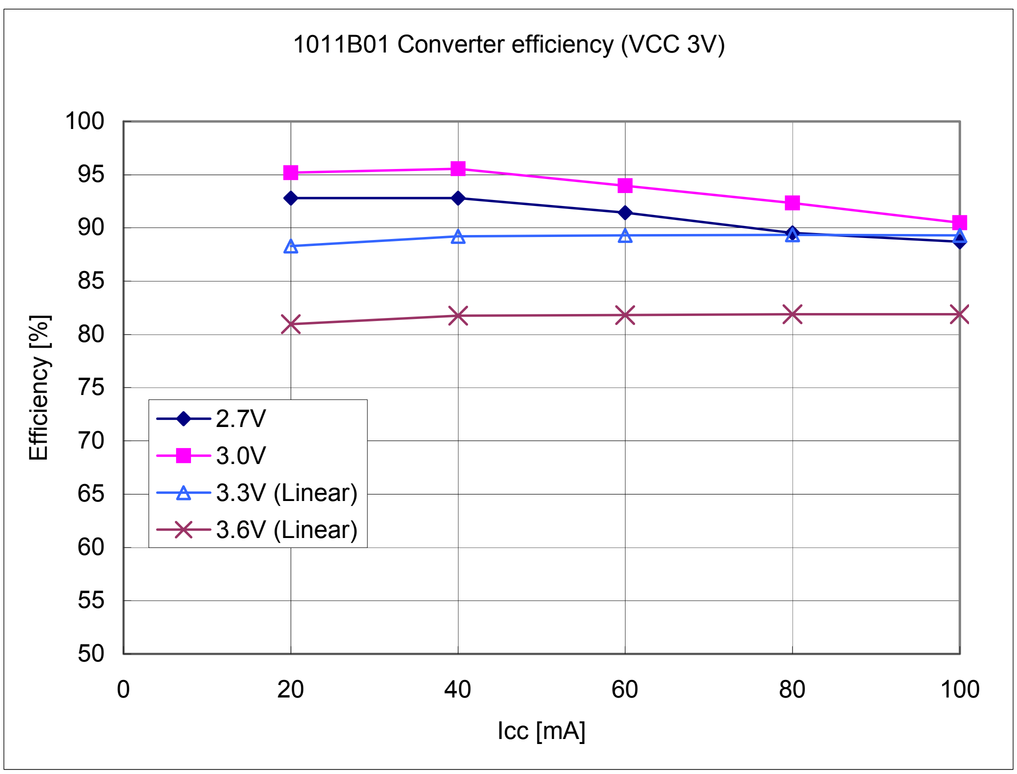


Figure 13: DC – DC Converter Efficiency (V_{CC} = 3 V)

Output current on V_{CC} at 3 V. Input voltage on V_{DD} at 2.7, 3.0, 3.3 and 3.6 volts.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Interface Requirements – Data Signals: I/O, AUX1, AUX2, and host interfaces: I/OUC, AUX1UC, AUX2UC. I_{SHORTL}, I_{SHORTH}, and V_{INACT} requirements do not pertain to I/OUC, AUX1UC, and AUX2UC. I_{IL} requirements only pertain to I//OUC, AUX1UC, and AUX2UC.						
V_{OH}	Output level, high (I/O, AUX1, AUX2)	I_{OH} = 0	0.9 V_{CC}		V_{CC}+ 0.1	V
		I_{OH} = -40 µA	0.75 V_{CC}		V_{CC} + 0.1	V
V_{OH}	Output level, high (I/OUC, AUX1UC, AUX2UC)	I_{OH} = 0	0.9 V_{DD}		V_{DD}+ 0.1	V
		I_{OH} = -40 µA	0.75 V_{DD}		V_{DD} + 0.1	V
V_{OL}	Output level, low	I_{OL}=1 mA			0.3	V
V_{IH}	Input level, high (I/O, AUX1, AUX2)		1.8		V_{CC} + 0.30	V
V_{IH}	Input level, high (I/OUC, AUX1UC, AUX2UC)		1.8		V_{DD} + 0.30	V
V_{IL}	Input level, low		-0.3		0.8	V
V_{INACT}	Output voltage when outside of session	I_{OL} = 0			0.1	V
		I_{OL} = 1 mA			0.3	V
I_{LEAK}	Input leakage	V_{IH} = V_{CC}			10	µA
I_{IL}	Input current, low	V_{IL} = 0, CS = 1			0.65	mA
		V_{IL} = 0, CS = 0			5	µA
I_{SHORTL}	Short circuit output current	For output low, shorted to V_{CC} through 33 Ω			15	mA
I_{SHORTH}	Short circuit output current	For output high, shorted to ground through 33 Ω			15	mA
t_R, t_F	Output rise time, fall times	For I/O, AUX1, AUX2, C_L = 80 pF, 10% to 90% For I/OUC, AUX1UC, AUX2UC, CL=50 pF, 10% to 90%			100	ns
t_{IR}, t_{IF}	Input rise, fall times				1	µs
R_{PU}	Internal pull-up resistor	Output stable for >200 ns	8	11	14	kΩ
FD_{MAX}	Maximum data rate				1	MHz
T_{FDIO}	Delay, I/O to I/OUC, I/OUC to I/O			20		ns
C_{IN}	Input capacitance				10	pF

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Reset and Clock for card interface, RST, CLK						
V_{OH}	Output level, high	I_{OH} = -200 µA	0.9 V_{CC}		V_{CC}	V
V_{OL}	Output level, low	I_{OL} = 200 µA	0		0.3	V
V_{INACT}	Output voltage when outside of a session	I_{OL} = 0			0.1	V
		I_{OL} = 1 mA			0.3	V
I_{RST_LIM}	Output current limit, RST				30	mA
I_{CLK_LIM}	Output current limit, CLK				70	mA
t_R, t_F	Output rise time, fall time	C_L = 35 pF for CLK, 10% to 90%			8	ns
		C_L = 200 pF for RST, 10% to 90%			100	ns
δ	Duty cycle for CLK, except for f=f_{XTAL}	C_L =35 pF, F_{CLK} ≤ 20 MHz	45		55	%

14.4 DC Characteristics: Digital Signals

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Digital I/O except for OSC I/O						
V_{IL}	Input Low Voltage		-0.3		0.8	V
V_{IH}	Input High Voltage		1.8		V_{DD} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2 mA			0.45	V
V_{OH}	Output High Voltage	I_{OH} = -1 mA	V_{DD} - 0.45			V
R_{OUT}	Pull-up resistor, $\overline{INT}$			20		kΩ
$\lvert I_{IL1} \rvert$	Input Leakage Current	GND < V_{IN} < V_{DD}	-5		5	µA
Oscillator (XTALIN) I/O Parameters						
V_{ILXTAL}	Input Low Voltage - XTALIN		-0.3		0.3 V_{DD}	V
V_{IHXTAL}	Input High Voltage - XTALIN		0.7 V_{DD}		V_{DD}+0.3	V
I_{ILXTAL}	Input Current - XTALIN	GND < V_{IN} < V_{DD}	-30		30	µA
f_{MAX}	Max freq. Osc or external clock				27	MHz
δin	External input duty cycle limit	$t_{R/F}$ < 10% f_{IN}, 45% < δ_{CLK} < 55%	48		52	%

14.5 DC Characteristics: Supply

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I_{DD}	Supply Current on V_{DD}	Linear mode, ICC=0 I/O, AUX1, AUX2=high		4.9		mA
		Step up mode, ICC=0 I/O, AUX1, AUX2=high		4.7		mA
I_{DD_PD}	Supply Current on V_{DD} in Power Down mode	PWRDN=1, Start/stop bit = 0 All digital inputs driven with a true logical 0 or 1		0.11	2.5	µA

14.6 DC Characteristics: I^2C Interface

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
SDA, SCL						
V_{IL}	Input Low Voltage		-0.3		0.3* V_{DD}	V
V_{IH}	Input High Voltage		0.7*V_{DD}		V_{DD} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA			0.40	V
C_{IN}	Pin capacitance				10	pF
I_{IN}	Output High Voltage	I_{OH} = -1 mA	V_{DD} - 0.45			V
T_F	Output fall time	C_L = 0 to 400 pF	20 + 0.1*C_L		250	ns
T_{SP}	Pulse width of spikes that are suppressed	Transition from valid logic level to opposite level			50	ns

14.7 Voltage / Temperature Fault Detection Circuits

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DDF}	V_{DD} fault – V_{DD} Voltage supervisor threshold	No external resistor on VDDF_ADJ pin	2.15		2.4	V
V_{CCF}	V_{CC} fault – V_{CC} Voltage supervisor threshold	V_{CC} = 5 V	4.20		4.6	V
		V_{CC}= 3 V	2.5		2.7	V
T_F	Die over temperature fault		115		145	°C

15 Mechanical Drawings

15.1 32-pin QFN

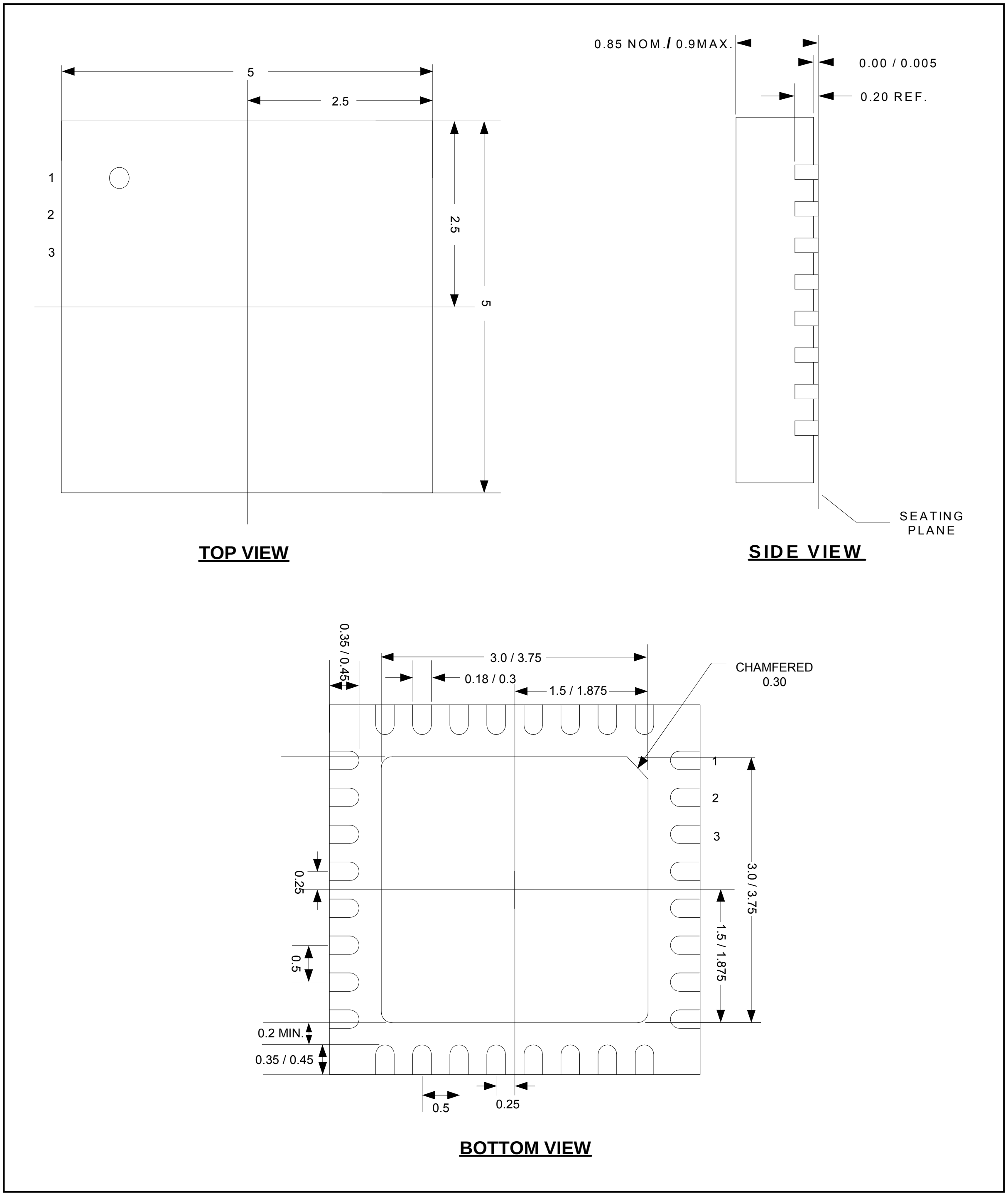


Figure 14: 32-pin QFN Package Drawing

15.2 28-pin SO

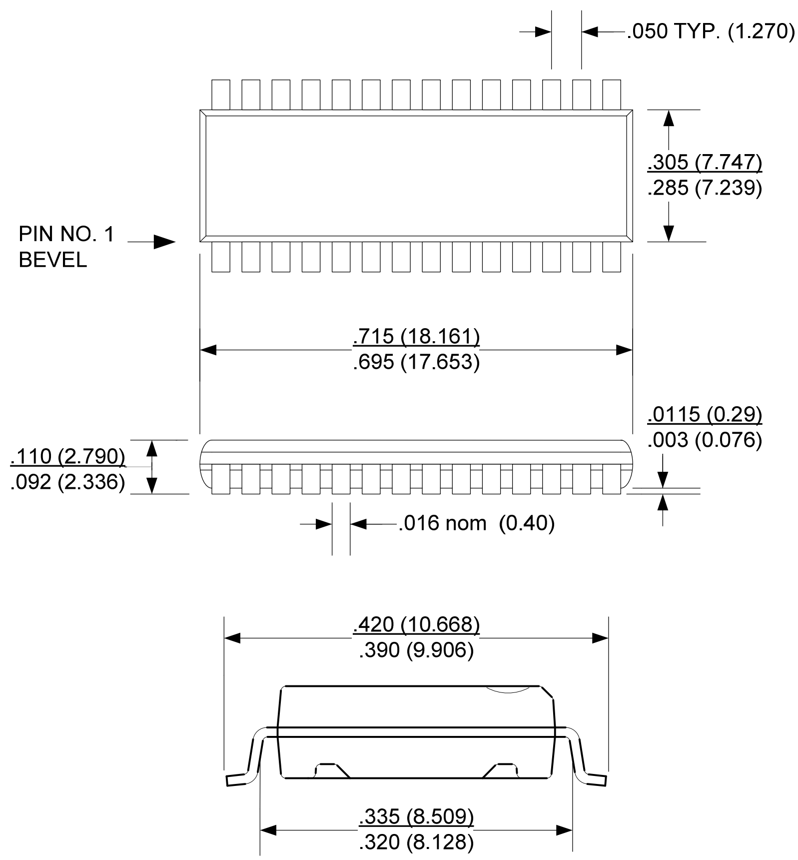


Figure 15: 28-pin SO Package Drawing

16 Package Pin Designation

Use handling procedures necessary for a static sensitive component.

16.1 32-pin QFN

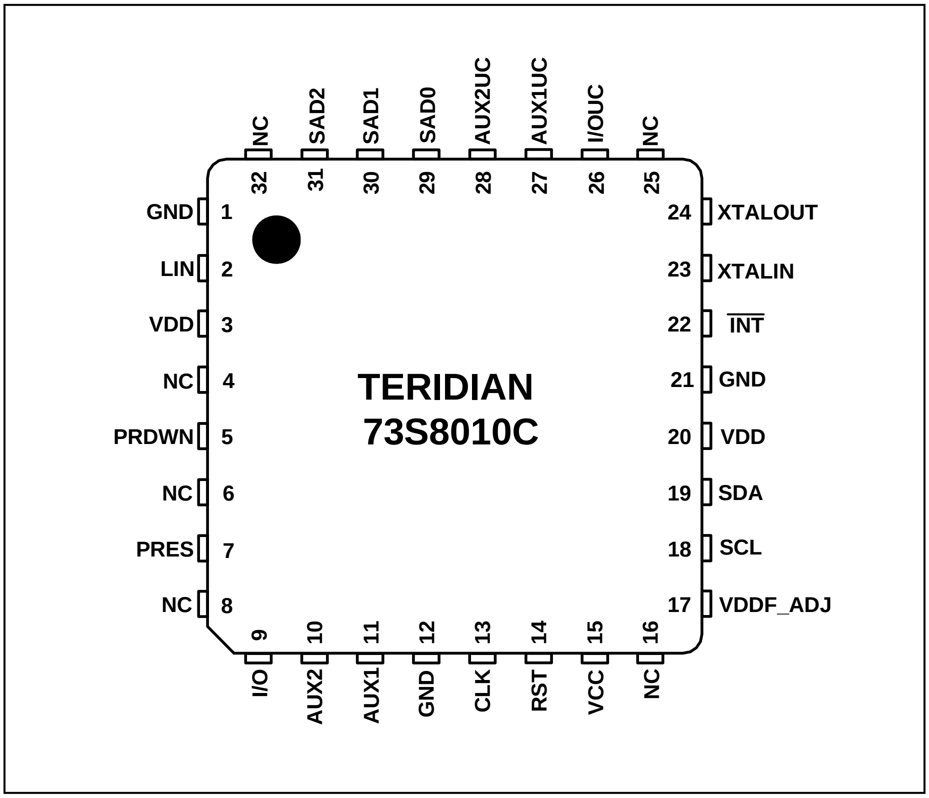


Figure 13: 73S8010C 32-pin QFN Pin Out

(Top View)

16.2 28-pin SO

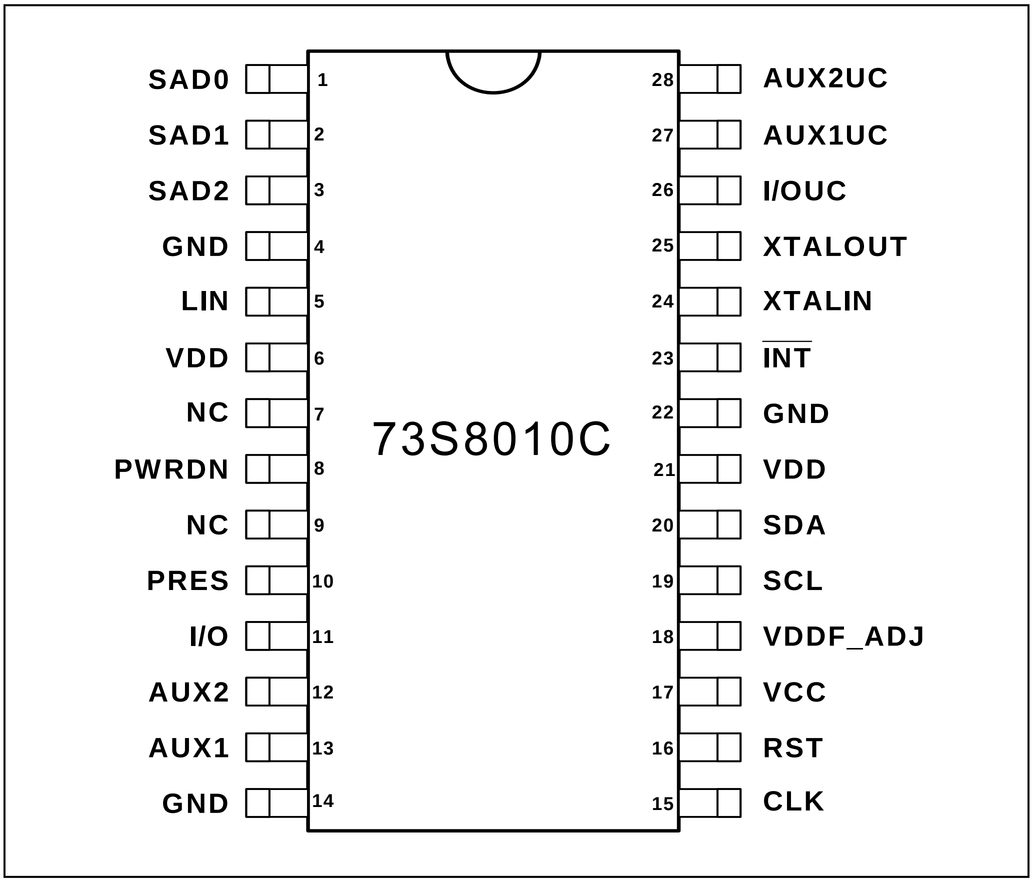


Figure 15: 73S8010C 28-pin SO Pin Out

(Top View)

17 Ordering Information

Part Description	Order Number	Packaging Mark
73S8010C-SO 28-pin Lead-Free SO	73S8010C-IL/F	73S8010C-IL
73S8010C-SO 28-pin Lead-Free SO Tape / Reel	73S8010C-ILR/F	73S8010C-IL
73S8010C-QFN 32-pin Lead-Free QFN	73S8010C-IM/F	73S8010C
73S8010C-QFN 32-pin Lead-Free QFN Tape / Reel	73S8010C-IMR/F	73S8010C

18 Related Documentation

The following 73S8010C documents are available from Teridian Semiconductor Corporation:

73S8010C Data Sheet (this document)
73S8010C 28SO Demo Board User's Guide
73S8010C QFN Demo Board User's Guide

19 Contact Information

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Revision History

Revision	Date	Description
1.0	6/13/2005	First publication.
1.2	9/21/2005	Changed SDATA hold time.
1.3	12/5/2007	Added ISO and ENV logo, remove leaded package options, replace 32QFN punched with SAWN, update 28SO dimension.
1.4	1/17/2008	Changed dimension of bottom exposed pad on 32QFN mechanical package figure.
1.5	4/3/2009	Removed all references to VPC as VPC must be tied to VDD.

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